Fri, 5 Jan 2007, 8:54:11 PM EST

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#9	((configure<in>metadata) <and> (control <in>metadata)) <and> (register<in>metadata)
#10	(~~Matthias Bauer~~<IN>metadata)
#11	(Bauer<IN>metadata)
#12	(((bauer<in>metadata))<AND>(ecker<in>metadata))
#13	(((bauer<in>metadata))<AND>(ecker<in>metadata))
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#16	(~~Matthias Bauer~~<IN>metadata)
#17	(~~Matthias Bauer~~<IN>metadata)
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1 Improving the performance of speculatively parallel applications on the Hydra CMP

Kunle Olukotun, Lance Hammond, Mark Willey

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: chip multiprocessor, data speculation, feedback-driven optimization, multithreading, parallel programming, performance evaluation

2 Shape-based retrieval and analysis of 3D models

Thomas Funkhouser, Michael Kazhdan

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(12.56 MB) Additional Information: full citation, abstract

Large repositories of 3D data are rapidly becoming available in several fields, including mechanical CAD, molecular biology, and computer graphics. As the number of 3D models grows, there is an increasing need for computer algorithms to help people find the interesting ones and discover relationships between them. Unfortunately, traditional text-based search techniques are not always effective for 3D models, especially when queries are geometric in nature (e.g., find me objects that fit into thi ...

3 Designers' forum: "cell" processor: An SPU reference model for simulation, random test generation and verification

Yukio Watanabe, Balazs Sallay, Brad Michael, Daniel Brokenshire, Gavin Meil, Hazim Shafi, Daisuke Hiraoka

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(265.87 KB) Additional Information: full citation, abstract, references

An instruction set level reference model was developed for the development of synergistic processing unit (SPU), which is one of the key components of the cell processor [1][2]. This reference model was used for the simulators to define the instruction set architecture (ISA), for the random test case generator, for the reference in the verification environment and for the software development. Using the same reference model for multiple purposes made it easier to keep up with the architecture ch ...

4 Automatic test pattern generation for functional RTL circuits using assignment

decision diagrams
Indradeep Ghosh, Masahiro Fujita
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(94.24 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present an algorithm for generating test patterns automatically from functional register transfer level (RTL) circuits that target detection of stuck-at faults in the circuit at the logic level. To do this we utilize a data structure named assignment decision diagram which has been proposed previously in the field of high level synthesis. The advent of RTL synthesis tools have made functional RTL designs widely popular. This paper addresses the problem of test patt ...

5 Parcel: project for the automatic restructuring and concurrent evaluation of LISP
L. Harrison
June 1988 **Proceedings of the 2nd international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.52 MB) Additional Information: full citation, abstract, references, citings, index terms

Parcel (Project for the Automatic Restructuring and Concurrent Evaluation of Lisp) is an investigation of the problem of compiling Lisp for evaluation on a shared memory multiprocessor. In this paper, we present an overview of the process of compilation in Parcel. This process consists, broadly, of an interprocedural analysis, followed by a function-level restructuring of the lambda expressions that constitute a program. We discuss both of these phases, and illustrate the steps of restructu ...

6 Proceedings of the SIGNUM conference on the programming environment for development of numerical software
March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1
Publisher: ACM Press
Full text available: pdf(5.02 MB) Additional Information: full citation

7 Efficient control flow quantification
Christoph Bockisch, Sebastian Kanthak, Michael Haupt, Matthew Arnold, Mira Mezini
October 2006 **ACM SIGPLAN Notices , Proceedings of the 21st annual ACM SIGPLAN conference on Object-oriented programming languages, systems, and applications OOPSLA '06**, Volume 41 Issue 10
Publisher: ACM Press
Full text available: pdf(245.83 KB) Additional Information: full citation, abstract, references, index terms

Aspect-oriented programming (AOP) is increasingly gaining in popularity. However, the focus of aspect-oriented language research has been mostly on language design issues; efficient implementation techniques have been less popular. As a result, the performance of certain AOP constructs is still poor. This is in particular true for constructs that rely on dynamic properties of the execution (e.g., the *cflow* construct).In this paper, we present efficient implementation techniques for *cfl* ...

Keywords: *aspect-oriented programming, control flow, virtual machine support*

8 Courses: State of the art in interactive ray tracing
Peter Shirley
July 2006 **Material presented at the ACM SIGGRAPH 2006 conference SIGGRAPH '06**
Publisher: ACM Press
Full text available: pdf(14.08 MB) Additional Information: full citation, abstract

Recent improvements in computer hardware have allowed ray tracing to be used in some interactive applications. The trends in architecture and expansions of geometric model should increase the use of interactive ray tracing. This course presents recent and often not-yet published work on interactive ray tracing.

9 Tools and methods for the verification of processors and processor-based systems: Smart diagnostics for configurable processor verification

Sadik Ezer, Scott Johnson

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(228.59 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a novel technique called Embedded Test-bench Control (ETC), extensively used in the verification of Tensilica's latest configurable processor. Conventional simulation-based verification methodologies that employ assembly programs for testing cannot easily link the diagnostic program to the test-bench for interactive control, consequently resulting in weaker coverage. ETC links the diagnostic program execution and the test-bench functions, thereby increasing the flexibility a ...

Keywords: configurable processors, coverage, diagnostics, embedded test-bench control, functional verification

10 Control CPR: a branch height reduction optimization for EPIC architectures

Michael Schlansker, Scott Mahlke, Richard Johnson

May 1999 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1999 conference on Programming language design and implementation PLDI '99**, Volume 34 Issue 5

Publisher: ACM Press

Full text available: pdf(2.06 MB) Additional Information: full citation, abstract, references, citings, index terms

The challenge of exploiting high degrees of instruction-level parallelism is often hampered by frequent branching. Both exposed branch latency and low branch throughput can restrict parallelism. *Control critical path reduction* (control CPR) is a compilation technique to address these problems. Control CPR can reduce the dependence height of critical paths through branch operations as well as decrease the number of executed branches. In this paper, we present an approach to control CPR tha ...

11 Novel ideas: Skipper: a microarchitecture for exploiting control-flow independence

Chen-Yong Cher, T. N. Vijaykumar

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.51 MB) Additional Information: full citation, abstract, references, citings Publisher Site

Although modern superscalar processors achieve high branch prediction accuracy, certain branches either are inherently difficult to predict or incur destructive interference in prediction tables, causing significant performance loss due to mispredictions. We propose a novel microarchitecture, called Skipper, to handle such difficult branches by exploiting control-flow independence. Previous approaches to handling difficult branches, one way or another, amount to executing incorrect instructions, ...

12 Multithreading and value prediction: Speculative lock elision: enabling highly concurrent multithreaded execution

Ravi Rajwar, James R. Goodman

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings
Publisher Site

Serialization of threads due to critical sections is a fundamental bottleneck to achieving high performance in multithreaded programs. Dynamically, such serialization may be unnecessary because these critical sections could have safely executed concurrently without locks. Current processors cannot fully exploit such parallelism because they do not have mechanisms to dynamically detect such false inter-thread dependences.We propose *Speculative Lock Elision (SLE),* a novel micro-architectura ...

13 The Clipper processor: instruction set architecture and implementation
W. Hollingsworth, H. Sachs, A. J. Smith
February 1989 **Communications of the ACM**, Volume 32 Issue 2
Publisher: ACM Press
Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

14 Experience Using Multiprocessor Systems—A Status Report
Anita K. Jones, Peter Schwarz
June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2
Publisher: ACM Press
Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

15 A survey of commercial parallel processors
Edward Gehringer, Janne Abullarade, Michael H. Gulyn
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

16 Experiences in functional validation of a high level synthesis system
Ranga Vemuri, Paddy Mamtora, Praveen Sinha, Nand Kumar, Jay Roy, Raghu Vutukuru
July 1993 **Proceedings of the 30th international conference on Design automation**
Publisher: ACM Press
Full text available: pdf(911.68 KB) Additional Information: full citation, references, citings, index terms

17 Design validation techniques: Semi-formal test generation and resolving a temporal abstraction problem in practice: industrial application
Julia Dushina, Mike Benjamin, Daniel Geist
January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**
Publisher: ACM Press
Full text available: pdf(130.37 KB) Additional Information: full citation, abstract, references

This document describes a successful application of a semi-formal test generation technique to the verification of Direct Memory Access Controller (DMAC) of ST50, a new

general purpose RISC microprocessor developed by STMicroelectronics and Hitachi. Like other memory-related devices, the DMA controller challenges formal techniques because of the state explosion problem. To cope with the challenge, abstraction mechanism is applied during test generation: several abstract models are created in ord ...

18 Moving towards more effective validation: A comparison of three verification techniques: directed testing, pseudo-random testing and property checking

Mike G. Bartley, Darren Galpin, Tim Blackmore

June 2002 **Proceedings of the 39th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(212.50 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the verification of two versions of a bridge between two on-chip buses. The verification was performed just as the Infineon Technologies Design Centre in Bristol was introducing pseudo-random testing (using Specman) and property checking (using GateProp) into their verification flows and thus provides a good opportunity to compare these two techniques with the existing strategy of directed testing using VHDL bus functional models.

19 Mondrian memory protection

Emmett Witchel, Josh Cates, Krste Asanović

October 2002 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , ACM SIGOPS Operating Systems Review , Proceedings of the 10th international conference on Architectural support for programming languages and operating systems ASPLOS-X**, Volume 37 , 30 , 36 Issue 10 , 5 , 5

Publisher: ACM Press

Full text available: pdf(1.53 MB) Additional Information: full citation, abstract, references, citings

Mondrian memory protection (MMP) is a fine-grained protection scheme that allows multiple protection domains to flexibly share memory and export protected services. In contrast to earlier page-based systems, MMP allows arbitrary permissions control at the granularity of individual words. We use a compressed permissions table to reduce space overheads and employ two levels of permissions caching to reduce run-time overheads. The protection tables in our implementation add less than 9% overhead to ...

20 Behavioral synthesis methodology for HDL-based specification and validation

D. Knapp, T. Ly, D. MacMillen, R. Miller

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(51.94 KB) Additional Information: full citation, references, citings, index terms

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